AMENDMENTS TO THE CLAIMS

Please cancel claims 9 and 24 without prejudice. Kindly amend claims 1, 22, 25 as shown in the following listing of claims. The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (currently amended) An Ethernet controller which processes packets received from a plurality of root complexes via a serial load/store fabric, the Ethernet controller comprising:

   a bus interface coupled to the serial load/store fabric, said bus interface associating each of the packets with their root complex; and

   control register logic, having a plurality of control registers, wherein each of said plurality of control registers is selectable to service at least one of the root complexes based on the association of the packets with their originating root complex;

   wherein the packets comprise:

   a PCI Express transaction layer packet (TLP); and

   a header, for associating said transaction layer packet with one of the root complexes.

2. (original) The Ethernet controller as recited in claim 1 wherein the Ethernet controller is a 1 Gig Ethernet controller.

3. (original) The Ethernet controller as recited in claim 1 wherein the Ethernet controller is a 10 Gig Ethernet controller.

4. (original) The Ethernet controller as recited in claim 1 wherein the serial load/store fabric utilizes the PCI Express specification.

5. (original) The Ethernet controller as recited in claim 1 wherein the serial load/store fabric is encapsulated within a second fabric.

6. (original) The Ethernet controller as recited in claim 5 wherein said second fabric is a channel based fabric.

7. (original) The Ethernet controller as recited in claim 6 wherein said second fabric comprises Advanced Switching.

8. (original) The Ethernet controller as recited in claim 6 wherein said second fabric comprises All Ethernet.

9. (canceled)

10. (original) The Ethernet controller as recited in claim 1 wherein the plurality of root complexes comprise a first computer executing a Microsoft Windows operating system.

11. (original) The Ethernet controller as recited in claim 10 wherein said Microsoft Windows operating system is unaware that it is sharing the Ethernet controller with any other of the plurality of root complexes.

12. (original) The Ethernet controller as recited in claim 10 wherein the plurality of root complexes further comprise a second computer executing a Linux operating system.

13. (original) The Ethernet controller as recited in claim 12 wherein said Linux operating system is unaware that it is sharing the Ethernet controller with said first computer.

14. (original) The Ethernet controller as recited in claim 1 wherein said bus interface comprises a table for associating each of said plurality of control registers with at least one of the plurality of root complexes.

15. (original) The Ethernet controller as recited in claim 14 wherein said table is used to select one of said plurality of control registers to be used to process each of the packets received by the Ethernet controller.

16. (original) The Ethernet controller as recited in claim 1 wherein said bus interface further comprises a multiplexer for selecting at least one of said plurality of control registers based on the associating performed by said bus interface.

17. (original) The Ethernet controller as recited in claim 1 wherein each of said plurality of control registers comprise:

a set of dedicated control registers; and

a set of shared or aliased control registers.

18. (original) The Ethernet controller as recited in claim 17 wherein said set of dedicated control registers are dedicated to a particular one of the plurality of root complexes.

19. (original) The Ethernet controller as recited in claim 17 wherein said set of shared or aliased control registers, support the plurality of root complexes.

20. (original) The Ethernet controller as recited in claim 1 further comprising:

a plurality of direct memory access (DMA) engines, each for handling packets from at least one of the plurality of root complexes; and

arbitration logic, coupled to said plurality of direct memory access engines, for arbitrating selection of said plurality of direct memory access engines used to process the packets received by the Ethernet controller from the plurality of root complexes.

21. (original) The Ethernet controller as recited in claim 20 wherein said arbitration logic selects a particular one of said plurality of direct memory access engines for processing of packets received from more than one of the plurality of root complexes.

22. (currently amended) A shared network interface controller comprising:

a bus interface to a serial load/store fabric; and

a plurality of control registers selectable by said bus interface to be associated with packets from a plurality of root complexes;

wherein said serial load/store fabric comprises PCI Express plus header information to associate each of said packets with an associated one of said plurality of root complexes.

23. The shared network interface controller as recited in claim 22 wherein said serial load/store fabric comprises PCI Express.

24. (canceled)

25. (currently amended) The shared network interface controller as recited in ~~claim 24~~ claim 22 wherein said bus interface is coupled to a shared I/O switch via said serial load/store fabric.

26. (original) The shared network interface controller as recited in claim 25 wherein said shared I/O switch places said header information within said packets.

27. (original) The shared network interface controller as recited in claim 22 wherein said bus interface comprises a lookup table for associating said plurality of control registers with said plurality of root complexes.

28. (original) The shared network interface controller as recited in claim 27 wherein said bus interface further comprises a multiplexer for selecting the plurality of control registers utilizing information within said lookup table.

29-59. (withdrawn)